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10/578,001	05/03/2006	Shunpei Yamazaki	740756-2967	3719

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EXAMINER	
KARIMY, MOHAMMAD TIMOR	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,001	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	MOHAMMAD Timor KARIMY	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/3/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-19, without traverse, in the reply filed on 02/15/2008 is acknowledged.

Product-by-Process Limitations

2. While not objectionable, the Office reminds applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, in re *Brown*, 173 USPQ 685; In re Luck, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re* Avery, 186 USPQ 161; *In re* Wethheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7 and 8 recite the limitation "**the** third conductive layer" in lines 16 and 16-17 respectively. There is insufficient antecedent basis for this limitation in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 10, 18, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al (US Pub. 2002/0089616 A1).

With respect to claim 1, Hashimoto discloses in figure 5, a thin film transistor comprising:

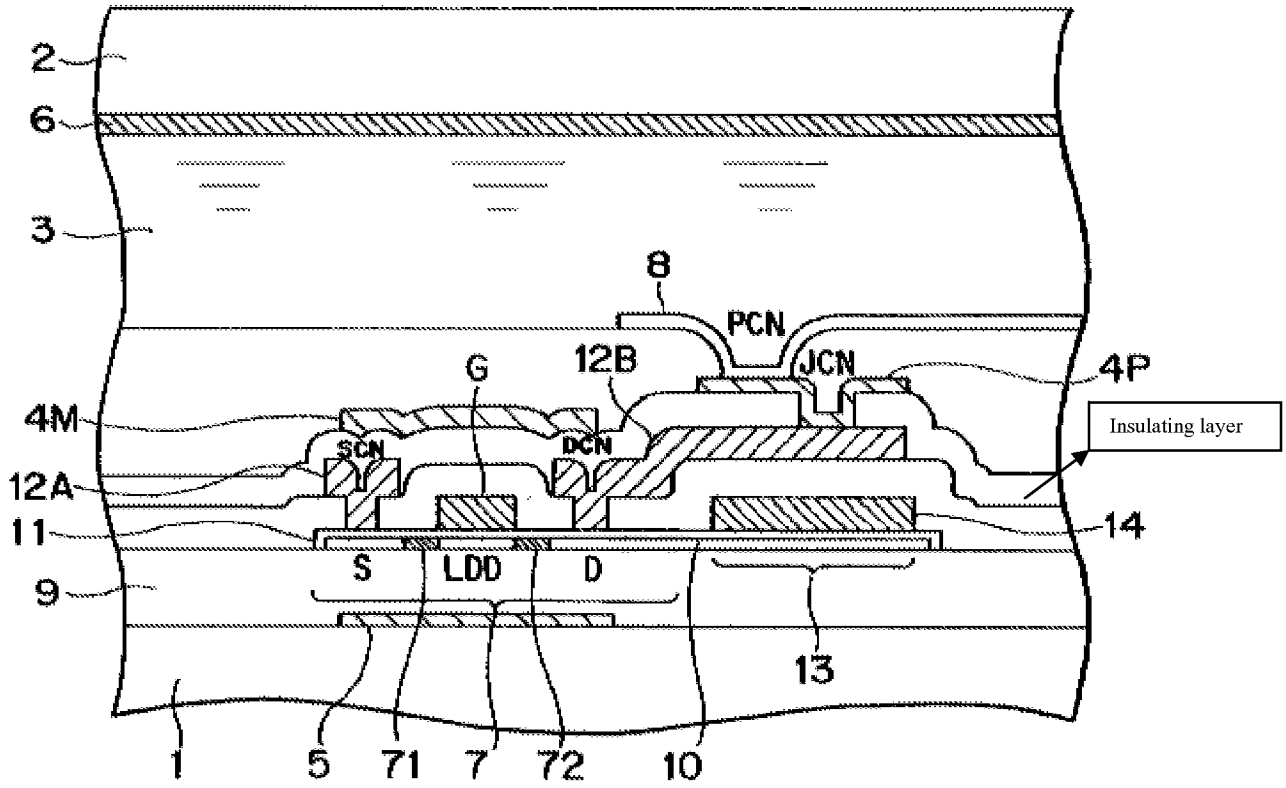
an insulating layer (see Fig. 5 below) having a first opening;

a first conductive layer 12B in the first opening;

a second conductive layer 4M on the first insulating layer and the first conductive layer 12B;

wherein the first conductive layer 12B is wider and thicker than the second conductive layer 4M.

FIG. 5



With respect to claim 10, Hashimoto implicitly teaches in Fig. 5 the thin film transistor of claim 1, wherein the thin film transistor further comprises a light shielding

film 5 below the first conductive layer 12B (Hashimoto teaches titanium as the material for a similar light shield film in Para [0005]).

With respect to claim 19, Hashimoto implicitly teaches in Fig. 5 the thin film transistor of claim 1, wherein a television apparatus can include the thin film transistor of claim 2.

Moreover, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

With respect to claim 2, Hashimoto discloses in figure 5, a thin film transistor comprising:

an insulating layer (see Fig. 5 above) having a first opening;

a first conductive layer 12B in the first opening;

a second conductive layer 4M on the first insulating layer and the first conductive layer 12B;

wherein the first conductive layer 12B is wider and thicker than the second conductive layer 4M.

The limitation "wherein the second conductive layer is formed by a droplet discharge method using a conductive material" is a product by process limitation, and it does not result to a structurally distinguishable product over Hashimoto's device. Moreover, the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

With respect to claim 3, Hashimoto discloses in figure 5, a display device comprising:

a first insulating layer 9 having a first opening;

a first conductive layer 5 in the first opening;

a second conductive layer 71 on the first insulating layer 9 and the first conductive layer 5;

a semiconductor layer (G & 14) over the second conductive layer 71 with a gate insulating film 11 there between;

a third conductive layer (12A) over the semiconductor layer (G & 14);

a second insulating layer having an opening over the third conductive layer; and

a fourth conductive layer 4P in the second opening;

wherein the first conductive layer 5 is wide and thicker than the second conductive layer 71,

wherein the fourth conductive layer 4P is thicker than the third conductive layer 12A.

With respect to claim 18, Hashimoto implicitly teaches in Fig. 5 the thin film transistor of claim 3, wherein a television apparatus can include the display device of claim 3.

Moreover, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed

apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

With respect to claim 4, Hashimoto discloses in figure 5, a display device comprising:

a first insulating layer 9 having a first opening;

a first conductive layer 5 in the first opening;

a second conductive layer 71 on the first insulating layer 9 and the first conductive layer 5;

a semiconductor layer (G & 14) over the second conductive layer 71 with a gate insulating film 11 there between;

a third conductive layer (12A) over the semiconductor layer (G & 14);

a second insulating layer having a second opening over the third conductive layer;

a fourth conductive layer 4P in the second opening;

wherein the first conductive layer 5 is wider and thicker than the second conductive layer 71,

wherein the fourth conductive layer 4P is thicker than the third conductive layer 12A.

The limitation “wherein each of the second conductive layer and the third conductive layer is formed by a droplet discharge method using a conductive material” is a product by process limitation, and it does not result to a structurally distinguishable

product over Hashimoto's device. Moreover, the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

7. With respect to claim 1 (second *U.S.C* ***102(b) rejection*** of claim 1), Hashimoto teaches in Fig. 2 a thin film transistor comprising:

an insulating layer 1 (quartz) having a first opening;

a first conductive layer 5 in the opening;

a second conductive layer 10 on the insulating layer and the first conductive layer, wherein the first conductive layer 5 is wider and thicker than the second conductive layer.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5-7, 8 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto in view of Poleshuk et al. (US Patent 4,389,481).

With respect to claim 5, Hashimoto discloses in figure 5, a display device comprising:

a first insulating layer 9 having a first opening;

a first conductive layer 5 in the first opening;

a second conductive layer 71 on the first insulating layer 9 and the first conductive layer 5;

a semiconductor layer (G & 14) over the second conductive layer 71 with a gate insulating film 11 there between;

a pair of third conductive layers (12A and 12B) over the semiconductor layer (G & 14);

a first electrode 8 over one of the pair of third conductive layers;

a second electrode 6 over the electroluminescent layer 3,

wherein the first conductive layer 5 is wider and thicker than the second conductive layer 71.

Though Hashimoto teaches a liquid crystal layer 3 over the first electrode 8; however, Hashimoto does not explicitly disclose electroluminescent material for this layer. Nonetheless, the use of electroluminescent material and liquid crystal are widely known to be used with TFTs in image display devices, and is understood to be art recognized equivalence. For instance, Poleshuk lists electroluminescent material and liquid crystal material as alternate materials used in image display devices. Therefore, it would have been obvious to a person of ordinary skill in the art to replace the liquid crystal layer of Hashimoto by an electroluminescent layer or vice versa as taught by Poleshuk.

With respect to claim 6, Hashimoto discloses in figure 5, a display device comprising:

a first insulating layer 9 having a first opening;

a first conductive layer 5 in the first opening;

a second conductive layer 71 on the first insulating layer 9 and the first conductive layer 5;

a semiconductor layer (G & 14) over the second conductive layer 71 with a gate insulating film 11 there between;

a pair of third conductive layers (12A and 12B) over the semiconductor layer (G & 14);

a first electrode 8 over one of the pair of third conductive layers;

a second electrode 6 over the electroluminescent layer 3,

wherein the first conductive layer 5 is wide and thicker than the second conductive layer 71.

Though Hashimoto teaches a liquid crystal layer 3 over the first electrode 8; however, Hashimoto does not explicitly disclose electroluminescent material for this layer. Nonetheless, the use of electroluminescent material and liquid crystal are widely known to be used with TFTs in image display devices, and is understood to be art recognized equivalence. For instance, Poleshuk lists electroluminescent material and liquid crystal material as alternate materials used in image display devices. Therefore, it would have been obvious to a person of ordinary skill in the art to replace the liquid

crystal layer of Hashimoto by an electroluminescent layer or vice versa as taught by Poleshuk.

Moreover, the limitation "wherein each of the second conductive layer and the third conductive layer is formed by a droplet discharge method using a conductive material" is a product by process limitation, and it does not result to a structurally distinguishable product over Hashimoto's device. Moreover, the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

With respect to claim 7, Hashimoto discloses in figure 5, a display device comprising:

a first insulating layer 9 having a first opening;

a first conductive layer 5 in the first opening;

a second conductive layer 71 on the first insulating layer 9 and the first conductive layer 5;

a semiconductor layer (G & 14) over the second conductive layer 71 with a gate insulating film 11 there between;

a pair of third conductive layers (12A and 12B) over the semiconductor layer (G & 14);

a first electrode 8 over one of the pair of third conductive layers;

a second insulating layer having an opening over the other one of the pair of third conductive layers;

a fourth conductive layer 4P in the second opening;

a second electrode 6 over the electroluminescent layer 3,

wherein the first conductive layer 5 is wide and thicker than the second conductive layer 71,

wherein the fourth conductive layer 4P is thicker than **the** third conductive layer 12A.

Though Hashimoto teaches a liquid crystal layer 3 over the first electrode 8 and under the second electrode 6; however, Hashimoto does not explicitly disclose electroluminescent material for this layer. Nonetheless, the use of electroluminescent material and liquid crystal are widely known to be used with TFTs in image display devices, and is understood to be art recognized equivalence. For instance, Poleshuk lists electroluminescent material and liquid crystal material as alternate materials used in image display devices. Therefore, it would have been obvious to a person of ordinary skill in the art to replace the liquid crystal layer of Hashimoto by an electroluminescent layer or vice versa as taught by Poleshuk.

With respect to claim 8, Hashimoto discloses in figure 5, a display device comprising:

a first insulating layer 9 having a first opening;

a first conductive layer 5 in the first opening;

a second conductive layer 71 on the first insulating layer 9 and the first conductive layer 5;

a semiconductor layer (G & 14) over the second conductive layer 71 with a gate insulating film 11 there between;

a pair of third conductive layers (12A and 12B) over the semiconductor layer (G & 14);

a first electrode 8 over one of the pair of third conductive layers;

a second insulating layer having an opening over the other one of the pair of third conductive layers;

a fourth conductive layer 4P in the second opening;

a second electrode 6 over the electroluminescent layer 3,

wherein the first conductive layer 5 is wide and thicker than the second conductive layer 71,

wherein the fourth conductive layer 4P is thicker than **the** third conductive layer 12A.

Though Hashimoto teaches a liquid crystal layer 3 over the first electrode 8 and under the second electrode 6; however, Hashimoto does not explicitly disclose electroluminescent material for this layer. Nonetheless, the use of electroluminescent material and liquid crystal are widely known to be used with TFTs in image display devices. For instance, Poleshuk lists electroluminescent material and liquid crystal material as alternate materials used in image display devices. Therefore, it would have been obvious to a person of ordinary skill in the art to replace the liquid crystal layer of Hashimoto by an electroluminescent layer or vice versa as taught by Poleshuk.

Furthermore, the limitation "wherein each of the second conductive layer and the third conductive layer is formed by a droplet discharge method using a conductive material" is a product by process limitation, and it does not result to a structurally distinguishable product over Hashimoto's device. Moreover, the method of forming a device is not germane to the issue of patentability of the device itself. Therefore, this limitation has not been given patentable weight.

With respect to claim 14, Hashimoto teaches in Fig. 5 the thin film transistor of claim 8, wherein the semiconductor layer is an amorphous semiconductor (Para [0002]).

With respect to claim 15, Hashimoto implicitly teaches in Fig. 5 the thin film transistor of claim 8, wherein the semiconductor layer is a semi-amorphous semiconductor (Para [0002]).

With respect to claim 16, Hashimoto implicitly teaches in Fig. 5 the thin film transistor of claim 8, wherein the semiconductor layer is a polycrystalline semiconductor (Para [0002]).

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto as applied to claim 1 above, and in view of Fujiwara et al. (US Patent 5,329,390).

With regard to claim 9, though Hashimoto implicitly teaches titanium as the material used for a light shield film; however, Hashimoto is silent about the use of titanium oxide. Nonetheless, titanium oxide is widely known to be used as one of the light shielding material optical devices. For instance, Fujiwara lists titanium oxide as

one of the material used in a light shielding layer (column 4 lines 19-27). As such, the use of titanium oxide would have been obvious to a person of ordinary skill in the art.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto as applied to claim 8 above, and in view of Tsai (US Pub. 2001/0014528 A1).

With respect to claim 12, though Hashimoto teaches aluminum as the material for the pair of third conductive layers; however, the use of aluminum and copper as alternative material in an interconnect structure is widely known in the semiconductor art. For example, Tsai discloses in Para [0029] the use of aluminum and copper as an alternate material in a conductive structure due to the metals' conductive properties. Therefore, the use of copper would have been obvious to one of ordinary skill in the art.

12. Claims 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto as applied to claim 8 above, and in view of Nakamura et al. (US Pub. 2001/0034088 A1).

With respect to claims 13 and 17, though Hashimoto does not disclose a range of from 5 to 100 μm for a channel width; however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to design a channel width between 5 to 100 μm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Moreover, these claimed dimensions are considered obvious to one of ordinary skill in the art in view Hashimoto. One of ordinary skill in the art is motivated to form device features as small as possible to be formed simultaneously on a single wafer, and with large enough thickness to allow proper device operation, in order to save on material and processing costs. As such, it would have been obvious to design a channel length from 5 to 100 μm.

Additionally, these claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688 (Fed. Cir.1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955)(selection of optimum ranges within prior art general conditions is obvious).

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto as applied to claim 1 above (Paragraph #7), and in view of Roberts et al. (US Patent 6,461,914 B1).

With respect to claim 11, though Hashimoto teaches the second conductive layer in Fig. 2 as indicated in claim a rejection; however, Hashimoto does not explicitly teach

copper as the material for the second conductive layer. However, the use of copper as the electrodes of a capacitor is commonly known in the semiconductor art. For instance, Roberts teaches the use of copper for the electrodes of capacitors in column 1 and lines 49-54. As such, the use of copper for capacitor electrodes would have been obvious to a person of ordinary skill in the art.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad Timor Karimy whose telephone number is 571-272-9006. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mtk

/Eugene Lee/
Primary Examiner, Art Unit 2815